

AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A system, comprising:
a bus;
a first random access memory (RAM);
a first memory testing engine (MTE) to execute test operations on the first random access memory;
a first bus controller for the bus, and in which the first memory testing is embedded integrated to have a first memory interface which is shared with the first memory testing engine to access the first RAM;
a second RAM;
a second MTE to execute test operations on the second RAM;
a second bus controller for the bus, and in which the second MTE is embedded to have a second memory interface which is shared with the second MTE to access the second RAM; and
a processor; and
~~a bus to connect the processor to the first bus controller wherein the first~~
~~wherein each~~ bus controller is to provide the processor access to the first random access memory via ~~the its respective~~ memory interface, and the processor is to control ~~the first~~
~~each~~ memory testing engine via the bus and the ~~first~~
~~respective~~ bus controller and wherein ~~the first~~
~~each~~ memory testing engine uses data, address and control pathways used by ~~the first~~
~~its respective~~ bus controller so that if data traffic from the processor is being passed to a memory module by the ~~first~~
~~respective~~ bus controller, ~~the first~~
~~its integrated~~ memory testing engine cannot run a test function.
2. (Canceled).
3. (Currently Amended) The system of claim 21, wherein the first and second memory testing engines can perform testing operations concurrently.
4. (Canceled).
5. (Previously Presented) The system of claim 1, wherein the first memory testing engine generates test data and expected responses.

6. (Previously Presented) The system of claim 5, wherein the first memory testing engine captures and compares an actual random access memory response to the test data.

7. (Previously Presented) The system of claim 1, wherein the first memory testing engine is responsible for programmable address ranges and data widths.

8. Canceled.

9. (Previously Presented) The system of claim 1 further comprising a register controller for the processor to configure the first memory testing engine.

Claims 10-11 (Canceled).

12. (Previously Presented) The system of claim 1, wherein the first memory testing engine saves a failing address for the processor.

13. (Previously Presented) The system of claim 1, wherein the first memory testing engine saves a failing data value for the processor.

14. (Previously Presented) The system of claim 1, wherein the first memory testing engine discontinues an active test until the processor reads a failing address and a memory address location.

15. (Previously Presented) The system of claim 1, wherein the first memory testing engine reports an asynchronous interrupt to the processor.

16. (Currently Amended) A method, comprising:
transmitting a plurality of initiation signals from a processor via a bus to a plurality of memory testing engines via a plurality of bus controllers,
respectively, for the bus;
testing a plurality of random access memories, respectively, using the plurality of initiated memory testing engines, respectively;
accessing from the processor through the bus the plurality of random access memories via the plurality of bus controllers, respectively;

accessing from the bus controllers the random access memories using a plurality of memory controllers, respectively; and
passing control of data, address and control pathways between (1) each one of the memory test engines, and (2) a respective one of the bus controllers, so that only one of the two has control at one time.

17. Canceled.
18. (Previously Presented) The method of claim 16, further comprising transmitting data traffic from the processor through the bus to one of the random access memories via the data, address and control pathways while such are under control of the respective bus controller.
19. (Original) The method of claim 16, further comprising generating test data and expected responses.
20. (Original) The method of claim 19, further comprising capturing and comparing an actual random access memory response to the test data.
21. (Previously Presented) The method of claim 16, wherein testing comprises writing multiple data patterns per memory location within a random access memory and comparing a reading of the location with an expected response.
22. Canceled.
23. (Previously Presented) The method of claim 16, further comprising: configuring the memory test engines using a plurality of register controllers, respectively.

Claims 24-25 (Canceled).

26. (Original) The method of claim 16, further comprising saving a failing address for the processor.
27. (Original) The method of claim 16, further comprising saving a failing data value for the processor.

28. (Original) The method of claim 16, further comprising discontinuing an active test until the processor reads a failing address and a memory address location.
29. (Original) The method of claim 16, further comprising reporting an asynchronous interrupt to the processor.
30. (Currently Amended) A machine-readable storage medium tangibly embodying a sequence of instructions executable by a machine to perform a method comprising:
accessing over a bus ~~a memory associated with an application specific integrated circuit (ASIC)~~ each of a plurality of memories that is associated with a respective one of a plurality of ASICS, via a respective one of a plurality of utility bus slave (UBS) controller controllers on the respective ASIC; configuring each of a plurality of memory test engine (MTE) engines (MTEs) that is embedded integrated in the respective UBS controller to have the same memory interface to said memory, by writing to a respective one of the UBS controller controllers over said bus; and processing a signal from each of the MTE-MTEs that a test of said its respective memory is complete.

Claims 31-33 (Canceled).

34. (Previously Presented) The machine-readable storage medium of claim 31, further comprising instructions that when executed control the capturing and comparing of an actual random access memory response to the test data.
35. (Currently Amended) The machine-readable storage medium of claim 30, wherein the instructions are such that the ~~testing-test~~ comprises writing multiple data patterns per memory location within the memory and comparing a reading of the location with an expected response.
36. (Currently Amended) The machine-readable storage medium of claim 30, further comprising instructions that when executed configure each of the MTE-MTEs by writing to a respective register controller.

37. (Previously Presented) The machine-readable storage medium of claim 30, further comprising instructions that when executed test memory in a decrementing memory address order.

Claims 38-39 (Canceled).

40. (Currently Amended) The machine-readable storage medium of claim 30, further comprising instructions that when executed save a failing address for ~~the-a~~ processor.

41. (Currently Amended) The machine-readable storage medium of claim 30, further comprising instructions that when executed save a failing data value for ~~the-a~~ processor.

42. (Previously Presented) The machine-readable storage medium of claim 30, further comprising instructions that when executed discontinue an active test until a processor reads a failing address and a memory address location.

43. (Previously Presented) The machine-readable storage medium of claim 30, further comprising instructions that when executed report an asynchronous interrupt to a processor.

44. (Currently Amended) An apparatus comprising:

first means for testing a first memory;

second means for testing a second memory wherein the first and second memory are to be tested at once by the first and second testing means;

first means for controlling a bus and accessing the first memory, the first testing means being embedded integrated in the first bus controlling means to share the same memory interface;

second means for controlling the bus and accessing the second memory, the second testing means being integrated in the second bus controlling means to share the same memory interface;

means for initiating the testing by the first and second testing means, by accessing the each testing means over the bus and via its respective bus controller means; and

means for disabling ~~the~~each testing means while passing data traffic from the initiating means to the respective memory over the bus.

Claims 45-46 (Canceled).

47. (Original) The apparatus of claim 44, further comprising a means for generating test data and expected responses.

48. (Original) The apparatus of claim 47, further comprising a means for capturing and comparing an actual random access memory response to the test data.

Claims 49-53 (Canceled).

54. (Previously Presented) The apparatus of claim 44, further comprising a means for saving a failing address for the initiation means.

55. (Previously Presented) The apparatus of claim 44, further comprising a means for saving a failing data value for the initiation means.

56. (Previously Presented) The apparatus of claim 44, further comprising a means for discontinuing an active test until the initiation means reads a failing address and a memory address location.

57. (Previously Presented) The apparatus of claim 44, further comprising a means for reporting an asynchronous interrupt to the initiation means.